REMARKS

It is noted the Official Action mailed December 29, 2003 crossed in the mail with Applicant's Amendment of December 26, 2003. Based on an interim telephone message from the Examiner, it is understood that the Examiner did not enter the Preliminary Amendment mailed December 26, 2003. Accordingly, this Amendment has been prepared with the understanding that the December 26, 2003 Preliminary Amendment has not been entered.

Fig. 3C has been amended to conform to the specification. No new matter has been entered.

Independent claim 37 has been amended to address the rejection under 35 USC § 112, second paragraph. Support is found in the specification, beginning at page 6. No new matter has been entered.

The art rejections are respectfully traversed. Considering first the rejection of independent claim 37 and dependent claims 39 - 41 as obvious from the admitted prior art (APA) in view of Gilbert, in rejecting the claims as obvious from the APA in view of Gilbert et al., the Examiner acknowledges that the APA does not teach forming a first photoresist pattern layer, a first photomask and forming a trench in the semiconductor substrate by an etching process using the first photoresist pattern layer. However, the Examiner takes the position that this missing teaching is provided by Gilbert et al. Even assuming arguendo Gilbert is as the Examiner suggests, the combination still would not achieve Applicant's claim 37, as amended. In Gilbert, the trench formed following the first etching step is filled with a non-conductive material (Column 2, lines 56-60). In Applicant's claimed invention, each of the dummy gate patterns has a reduced area of a respective one of the dummy area patterns. Gilbert et al. does not teach

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forming each of the dummy gates patterns with a reduced area of a respective one of the dummy area patterns as required by independent claim 37 of the instant Application. Nowhere does Gilbert et al. teach or suggest using a first masking layer defining a trench which partitions pattern areas corresponding to active regions and dummy regions, using that masking layer in an etching step to form trenches in the semiconductor substrate which partitions dummy area patterns from the active area patterns, removing the first masking layer, burying insulating layers in the trenches after the first masking layer is removed forming a conductive layer on the semiconductor substrate, and then using a second masking layer to form dummy gates having a reduced area corresponding to the dummy area patterns as required by Applicant's independent claim 37. Thus, Gilbert et al. cannot be combined with the Applicant's APA to render obvious claim 37 or claims 39-40 which depend thereon.

The rejection of claim 41 has been rendered moot by its cancellation.

Turning to the rejection of claim 38 as obvious from the APA in view of Gilbert et al. and further in view of Shimomura et al. (U.S. Patent No. 6,140,687), claim 38 is dependent on claim 37. The deficiencies of the combination of the APA and Gilbert et al. vis-à-vis claim 37 are discussed above. It is not seen that Shimomura et al. supplies the missing teachings to the APA/Gilbert et al. combination to achieve or render obvious claim 37, or claim 38 which depends thereon. Shimomura et al. has been cited specifically to teach that it is conventional to form circular shaped gates. Even assuming *arguendo* the Examiner's characterization of Shimomura et al., the more basic and essential teachings missing from the APA/Gilbert et al. combination, as discussed above, are not supplied by Shimomura et al. Thus, no combination of

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the APA, Gilbert et al. and Shimomura et al. could achieve or render obvious claims 37 or 38 which depends thereon.

New claims 42-47 are similarly allowable over the art.

Having dealt with all the objections raised by the Examiner, it is believed that the Application now is in order for allowance. Early and favorable action are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,

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CERTIFICATE OF MAILING

I certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" on March 25, 2004 at Tucson, Arizona.

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Fig. 3A PRIOR ART

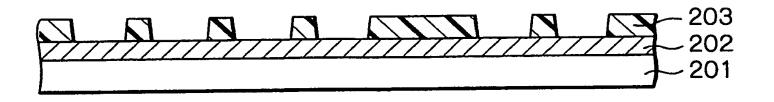


Fig. 3B PRIOR ART

